

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled).

Claim 2 (currently amended): An integrated circuit, comprising:

a scan path having an input and an output;

a pin coupled to the input and the output of the scan path, ~~The integrated circuit of claim 1~~
wherein:

~~a first the I/O pin is operable to input~~ inputs scan test data to the scan path at a first test time; and

~~the first I/O pin is operable to output~~ outputs scan test data from the scan path at a second test time.

Claim 3 (currently amended): An integrated circuit, comprising:

a first scan path;

a second scan path;

~~the a first I/O pin is operable to input~~ inputting input scan test data to ~~[[a]]~~ an input of the
first scan path at the a first test time and outputting output scan test data from an output of
the second scan path at a second test time; and

~~a second I/O pin is operable to input~~ inputting input scan test data to ~~[[a]]~~ an input of the
second scan path at the first test time and outputting output scan test data from an output
of the first scan path at the second test time. ;

~~the first I/O pin is operable to output scan test data from the second scan path at the second~~
~~test time; and~~

~~the second I/O pin is operable to output scan test data from the first scan path at the second~~
~~test time.~~

Claim 4 (currently amended): The integrated circuit of claim 3, wherein at least one of the first scan path and the second scan path further comprises a series of scan paths.

Claim 5 (currently amended): The integrated circuit of claim 2, ~~further comprising~~ wherein the scan path comprises a series of scan paths, ~~wherein:~~

~~the first I/O pin is operable to input scan test data to the series at a first test time; and~~

~~the first I/O pin is operable to output scan test data from the series at a second test time.~~

Claim 6 (currently amended): The integrated circuit of claim 2, further comprising functional circuitry, wherein ~~[[:]]~~ the scan path interacts with the functional circuitry, ~~[[:]]~~

~~the first I/O pin is operable to input scan test data at the first test time; and~~

~~the first I/O pin is operable to output scan test data at the second test time.~~

Claim 7 (currently amended): The integrated circuit of claim 2, further comprising functional circuitry, wherein:

~~the first I/O pin is operable to input~~ inputs functional test data to the functional circuitry ~~at the first a third~~ test time; and

~~the first I/O pin is operable to output~~ outputs functional test data from the functional circuitry ~~at the second a fourth~~ test time.

Claims 8 to 11 (canceled).

Claim 12 (currently amended): An integrated circuit, comprising: ~~[[:]]~~

a functional circuit ~~operable to produce~~ producing functional output;

an I/O pin ~~operable to be used~~ that acts as input at a first time and as output at a second time, the I/O pin having a respective scan path ~~operable to produce~~ that produces scan output;

an I/O circuitry, comprising:

an input buffer coupled to (1) the I/O pin to receive input signal and (2) to the functional circuit to provide the input signal;

a virtual pin output buffer coupled to the I/O pin to provide output; and

a virtual pin multiplexer coupled to (1) the function circuit to receive the functional output and (2) the scan path to receive the scan output, the virtual pin multiplexer providing a virtual pin multiplexer output;

a virtual pin flip-flop coupled to the I/O pin and to the functional circuit and to the scan path (1) the virtual pin multiplexer to receive the virtual pin multiplexer output and (2) the virtual pin output buffer to provide the virtual pin multiplexer output, the virtual pin flip-flop operable to hold holding the functional output or the scan output received data for a clock cycle.

Claim 13 (currently amended): The integrated circuit of claim 12, further comprising:

a number of scan paths;

the same number of I/O pads pins; and

the same number of I/O circuitries, wherein and the same number of virtual pin flip-flops operable to form forms at least one register.

Claim 14 (currently amended): The integrated circuit of claim 13, wherein:

~~each I/O pad further comprises a scan output buffer;~~

each virtual pin flip-flop further comprises: [[:]]

a compact-control signal;

an output-data signal; and

an and-gate operable to eliminate receiving the compact-control signal and the output-data signal to eliminate don't-care data; and

the register is ~~operable as~~ a compaction register.

Claim 15 (currently amended): The integrated circuit of claim 13, wherein:

each I/O ~~circuitry pad~~ further comprises: [[:]]

a reseed multiplexer operable to receive receiving (1) the scan functional output data from the scan path and (2) scan input derived from the input buffer, the reseed multiplexer providing the scan output or the scan input to the virtual pin

multiplexer data; and

a reseed control signal ~~operable to control~~ controlling the reseed multiplexer; and

the register is ~~operable as~~ a reseed register.

Claim 16 (currently amended): The integrated circuit of claim ~~[[15]]~~ 13, wherein:

each I/O ~~pad~~ circuitry further comprises:

an XOR-gate operable to receive input from the output of coupled to receive a linear feedback shift register (LFSR) input and a LFSR feedback, the XOR-gate providing an XOR-gate output; and

a reseed multiplexer coupled to receive (1) the XOR-gate output and (2) scan input, the reseed multiplexer providing a reseed multiplexer output;

a reseed flip-flop coupled to receive the reseed multiplexer output, the reseed flip-flop providing a reseed flip-flop output; and

an input multiplexer coupled to receive the input signal and the reseed flip-flop output, the input multiplexer generating the scan input.

~~the register is operable as a linear feedback shift register.~~

Claim 17 (currently amended): The integrated circuit of claim 13, further comprising a second number of flip-flops ~~operable to form~~ that form a compaction register, wherein:

~~the integrated circuit is operable to perform~~ performs reseeding and compaction at the same time. ; and

~~the integrated circuit is at the same time operable to perform compaction.~~

Claim 18 (currently amended): The integrated circuit of claim 17, wherein the compaction register ~~can be~~ is read serially.

Claim 19 (currently amended): A method, comprising:

inputting scan data to an I/O pin during a first time;

processing the scan data in a respective scan path to produce scan output data; and

outputting the scan output data to the I/O pin at a second time.

Claim 20 (currently amended): The method of claim 19, further comprising:

multiplexing output data and scan output data; and

storing the output data or the scan output data in a flip-flop during the first time.

Claim 21 (currently amended): The method of claim 20, further comprising:

connecting a number of flip-flops associated with I/O pins; and

forming a register for performing a reseed test.

Claim 22 (currently amended): The method of claim 21, wherein forming a register further comprises:

sending a compact control signal;

and-gating the compact control signal with the output data;

eliminating don't care data; and

performing compaction.

Claim 23 (currently amended): The method of claim 21, wherein forming a register further comprises:

sending a reseed control signal to a reseed multiplexer;

multiplexing functional output data and scan input data; and

performing the reseed test.

Claim 24 (currently amended): The method of claim 23, wherein multiplexing further comprises:

receiving gated input from a linear feedback shift register; and

performing a linear feedback shift register reseed test.

Claim 25 (currently amended): The method of claim 19, wherein the first time and the second time occur during the same clock cycle.

Claim 26 (new): The integrated circuit of claim 12 further comprising:

an output buffer coupled to (1) the functional circuit to receive the functional output and
(2) the I/O pin to provide the functional output.